IN THE CLAIMS

1. (Original) An apparatus for performing adaptive frame tracking, comprising an adaptive frame tracking unit capable of receiving and sending at least one data packet and automatically adjusting a data rate of said data packet by determining if there exists at least one data frame error and correcting for said data frame error in response to a determination that there exists at least one said data frame error.

2. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit receives and sends at least one universal serial bus data packet.

3. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit is capable of receiving a frame of data from a computer peripheral device and perform adaptive frame tracking upon said frame of data and transmitting said frame of data.

4. (Currently amended) The apparatus of claim [[1]] 3, wherein said computer peripheral device is one of a computer modem, a scanner, a multimedia system, a computer mouse, and an external data read/write device.

5. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit is capable of receiving a frame of data from a universal serial bus host and performing adaptive frame tracking upon said frame of data and transmitting said frame of data.

6. (Currently amended) The apparatus of claim [[1]] 3, wherein said universal serial bus host is a computer system.

7. (Original) The apparatus of claim 1, wherein said data frame error further comprises a missing start of scan data pattern.

8. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit comprises:

a start of frame synthesizer circuit for monitoring data streams and determining whether there exists a start of frame data packet and performing a start of frame synthesis in response to a determination that a start of scan does not exist;

a frame position monitor circuit coupled with said start of frame synthesizer for generating a frame position monitor sample clock and a latched frame count signal;

an auto data rate control circuit, said auto data rate control circuit being coupled with said start of frame synthesizer circuit and said frame position monitor circuit, for generating a data packet size signal to determine a number of bytes to be received in said data frame; and

a frame number monitor circuit, said frame number monitor circuit being coupled with each of said start of frame synthesizer circuit, said frame position monitor circuit, and said auto data rate control circuit, for determining a present data frame number value and generating a time stamp match signal for determining whether a

frame number corresponding to a data frame that has a missing start of frame data packet.

9. (Original) The apparatus of claim 8, wherein said adaptive frame tracking unit is capable of performing adaptive synchronization.

10. (Original) The apparatus of claim 8, wherein said start of frame data packet comprises of a sync data field, a packet identification data field, a frame number field, a CRC5 bit, and an end of packet data field.

11. (Original) The apparatus of claim 8, wherein said start of frame synthesizer circuit comprises:

a frame counter for generating at least one data frame signal;

an error counter electronically coupled with said frame counter for generating a start of frame status signal; and

a set of digital logic electronically coupled with said frame counter and said error counter for generating at least one said data frame signal and said frame status signal.

12. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of tracking a number of bits in a frame of data.

13. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of detecting a missing start of frame data pattern.

14. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of performing a start of frame synthesis.

15. (Original) The apparatus of claim 11, wherein said data frame signal further comprises of a frame count signal.

16. (Original) The apparatus of claim 11, wherein said frame status signal further comprises of a synthesized start of frame signal.

17. (Original) The apparatus of claim 11, wherein said frame status signal further comprises of a missed start of frame signal.

18. (Currently amended) The apparatus of claim 8, wherein said frame position monitor circuit further comprises:

a[[n]] dividing counter for dividing at least one clock signal;

a frame count register logically coupled with said clock signal for latching a frame count signal; and

a set of digital logic electronically coupled with said dividing counter and said frame count register for generating said clock signal and latching said frame count signal.

19. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of performing a start of frame mastership.

20. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a frame position monitor sample clock.

21. (Original) The apparatus of claim 20, wherein said frame position monitor circuit is capable of dividing said frame position monitor sample clock by a plurality of values.

22. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a frame position updated signal.

23. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a latch frame count signal.

24. (Original) The apparatus of claim 8, wherein said auto rate control circuit further comprises:

an auto rate counter for generating a data frame count value;

an auto rate register for latching said data frame count value generated by said auto rate counter;

an auto rate controller for controlling said auto rate counter and said auto rate register; and

a left-shifter multiplier for multiplying a latched data frame count value by one of a plurality of values.

25. (Original) The apparatus of claim 24, wherein said auto rate control circuit is capable of controlling a data rate of an data endpoint.

26. (Original) The apparatus of claim 25, wherein said data endpoint is an isochronous data endpoint.

27. (Original) The apparatus of claim 24, wherein said auto rate control circuit is capable of generating a data packet size signal.

28. (Original) The apparatus of claim 27, wherein said data packet size signal is an isochronous packet size signal.

29. (Original) The apparatus of claim 28, wherein said auto rate control circuit is capable of sending said isochronous packet size signal to a data endpoint.

30. (Original) The apparatus of claim 24, wherein said auto rate counter is incremented by said auto rate controller using a frame position sample monitor clock.

31. (Original) The apparatus of claim 24, wherein said auto rate controller is capable of clearing and re-enabling said auto rate counter.

32. (Original) The apparatus of claim 8, wherein said frame number monitor circuit further comprises:

a frame number monitor counter for latching a frame number signal and generating a latched frame number monitor signal;

a time stamp match register for generating a time stamp match signal using said latched frame number monitor signal; and

a set of digital logic electronically coupled with said frame number monitor counter and said time stamp match register for latching said frame number signal and generating a time stamp match signal.

33. (Original) The apparatus of claim 32, wherein said frame number monitor counter increments said latched frame number signal in response to an assertion of a missed start of frequency signal.

34. (Original) The apparatus of claim 32, wherein said frame number monitor circuit generates said time stamp match signal in response to a determination that said latched frame number signal is one of equal to and greater than a time stamp match value signal.

35. (Original) The apparatus of claim 32, wherein said latched frame number monitor signal contains a universal serial bus frame number value.

36. (Original) The apparatus of claim 32, wherein said time stamp match register can be loaded with data using a software control.

37. (Currently amended) A method [[of]] for performing adaptive frame tracking, comprising:

monitoring at least one data packet from a data stream;

supporting transmit data buffering of said data packet;

determining whether at least one data packet is missing from a received data stream;

establishing a start of frame rate control for said data packet for said missing data packet; and

supporting an auto rate control of said data packet.

38. (Original) The method of claim 37, wherein receiving and sending at least one data packet from a data stream further comprises receiving universal serial bus isochronous data packets.

39. (Original) The method of claim 37, wherein determining whether at least one data packet is missing from a received data stream further comprises performing start of frame error checking.

40. (Original) The method of claim 37, wherein supporting an auto rate control of said data packet further comprises automatically adjusting a data rate of said data packets to match a data rate of a universal serial bus communication system.

41. (Original) An apparatus for performing adaptive frame tracking, comprising:

means for receiving and sending at least one data packet from a data stream;

means for supporting transmit data buffering of said data packet;

means for determining whether at least one data packet is missing from a received data stream;

means establishing a start of frame rate control for said data packet for said missing data packet; and

means for supporting an auto rate control of said data packet.